

AN11053

Ethernet throughput on the NXP ARM microcontrollers

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Application note

Document information

Info	Content
Keywords	LPC1700, Ethernet, ARM7, ARM9, Cortex-M3
Abstract	This application note discusses 3 different scenarios for measuring Ethernet Throughput on the LPC1700 product and details what is really achievable in an optimized system.

Revision history

Rev	Date	Description
1	20110323	Initial version.

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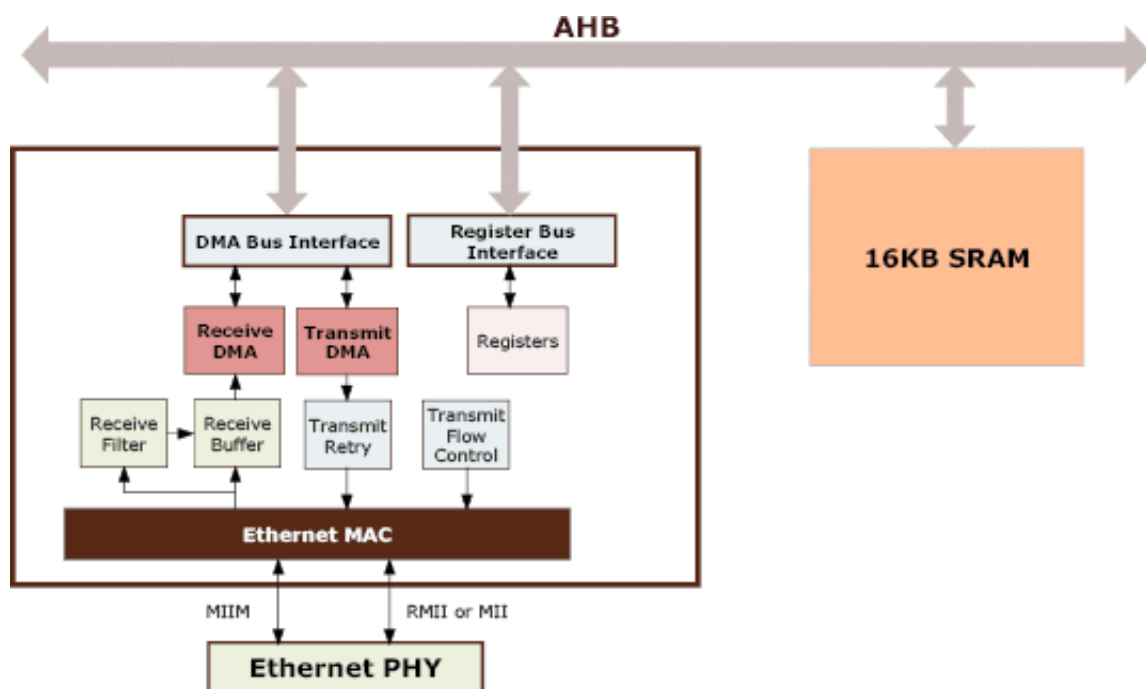
1. Introduction

Ethernet is the most widely-installed Local Area Network (LAN) technology in the world. It's been in use since the early 1980s and is covered by the IEEE standard 802.3, which specifies a number of speed grades. In embedded systems, the most commonly used format runs at both 10 Mbit/s and 100 Mbit/s (and is often referred to as 10/100 Ethernet).

There are more than 20 NXP ARM MCUs with built-in Ethernet, covering all three generations of ARM (ARM7, ARM9, and the Cortex-M3). NXP uses essentially the same implementation across all three generations, so designers can save time and resources by reusing their Ethernet function when systems move to the next generation of ARM.

1.1 Superior implementation

NXP's Ethernet block (see [Fig 1](#)) contains a full-featured 10/100 Ethernet MAC (media access controller) that uses DMA hardware acceleration to increase performance. The MAC is fully-compliant with IEEE standard 802.3 and interfaces with an off-chip Ethernet PHY (physical layer) using the MII (Media Independent Interface) or RMII (Reduced MII) protocol along with the on-chip MIIM (Media Independent Interface Management) serial bus.



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Fig 1. LPC24xx Ethernet block

The NXP Ethernet block is distinguished by the following:

- Full Ethernet Functionality

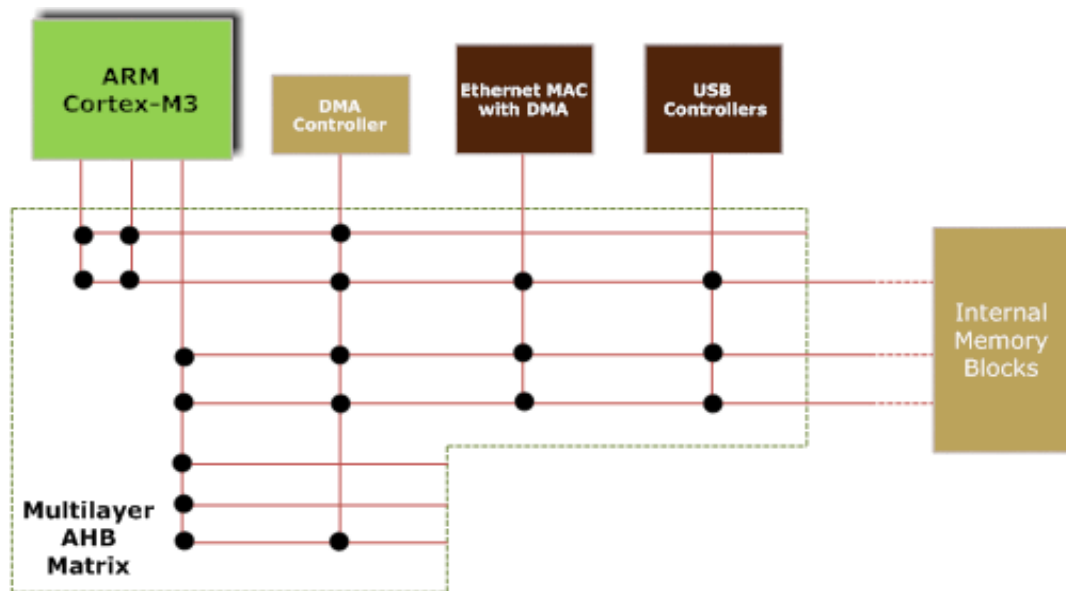
The block supports full Ethernet operation, as specified in the 802.3 standard.

- Enhanced Architecture

NXP has enhanced the architecture with several additional features including receive filtering, automatic collision back-off and frame retransmission, power management via clock switching, and more.

- DMA Hardware Acceleration

The block has two DMA managers, one each for transmit and receive. Automatic frame transmission and reception with Scatter-Gather DMA offloads the CPU even further.



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Fig 2. NXP's Cortex-M3 architecture

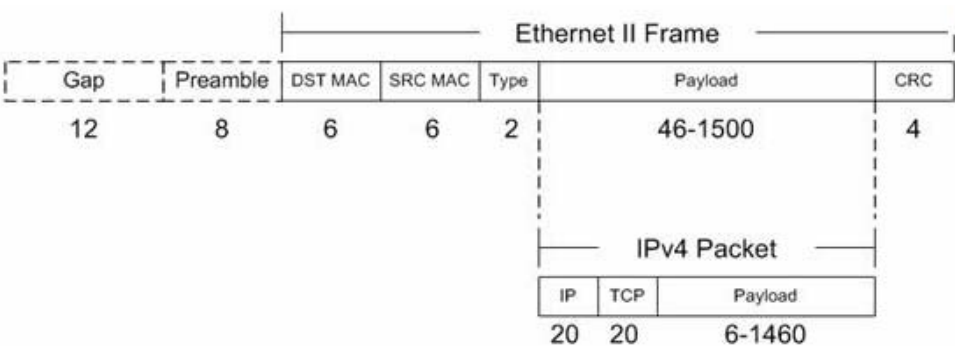
2. Ethernet throughput in NXP’s LPC1700 microcontrollers

In an Ethernet network, two or more stations send and receive data through a shared channel (a medium), using the Ethernet protocol. Ethernet Performance could mean different things for each of the network’s elements (channel or stations). Bandwidth, Throughput, and Latency are measures that contribute to the overall performance. In the case of the channel, while the Bandwidth is a measure of the capacity of the link, the Throughput is the rate at which usable data can be sent over the channel. In the case of the stations, the Ethernet performance could mean the ability of that equipment to operate at the full bit and frame rate of the Ethernet channel. On the other hand, Latency measures the delay in time caused by several factors (propagation times, processing times, faults, retries, etc).

The focus of this application note will be on the ability of the NXP LPC1700 to operate at the full bit and frame rate of the Ethernet channel to which it is connected, via the Ethernet interface (provided by the internal EMAC module plus the external PHY chip). In this way, the Throughput will be defined as a measure of usable data (payload) per second, which the MCU is able to send/receive to/from the communication channel. The same concepts can also be applied to other NXP LPC microcontrollers supporting Ethernet.

Unfortunately, these kinds of tests generally require specific equipment such Network Analyzers and/or Network Traffic Generators, in order to get precise measurements. Nevertheless, using simple test setups it is possible to get estimated numbers. In fact, our goal is to understand the different factors that can affect the Ethernet Throughput, so users can focus on different techniques in order to improve Ethernet performance.

Here the Throughput of the Transmitter is only considered; the Receiver is a little bit more complex because its performance is relative to the performance of the Transmitter that put the information into the channel (in this case, the throughput of the receiver will be affected by the throughput of the transmitter sending the data over the channel). Once we get the throughput for the transmitter, we could consider this number as the maximum ideal number that the receiver will be able to achieve (under ideal conditions), and get the throughput for the receiver relative to this number.



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Fig 3. Ethernet II frame

Considering a bit rate of 100 Mbit/s, and that every frame consists on the payload (useful data, minimum 46 B and maximum 1500 B), the Ethernet header (14 B), the CRC (4 B), Preamble (8 B) and the Inter-Packet Gap (12 B), then the following are the Maximum Possible Frames per Second and Throughput;

For minimum-sized frames: (46 B of Data) -> 148809 frame/s -> 6.84 MB/s

For maximum-sized frames: (1500 B of Data) -> 8127 frame/s -> 12.19 MB/s

The above rates are the Maximum Possible values which are in reality “impossible to reach”; that is, those values are “Ideal” and any practical implementation will have lower values.

Notes:

- Frame/s is calculated dividing the Ethernet Link speed (100 Mbit/s) by the total frame size in bits ($84 \times 8 = 672$ for minimum-sized frames, and $1538 \times 8 = 12304$ for Maximum-sized frames).
- MB/s is calculated multiplying the frames/s by the number of bytes of useful data in each frame (46 B for minimum-sized frames, and 1500 B for Maximum-sized frames).

2.1 Test conditions

MCU: LPC1768 running at 100 MHz

Board: Keil MCB1700

PHY chip: National DP83848 (RMII interface)

Tool Chain: Keil uVision4 v4.1

Code running from RAM

TxDescriptorNumber = 3

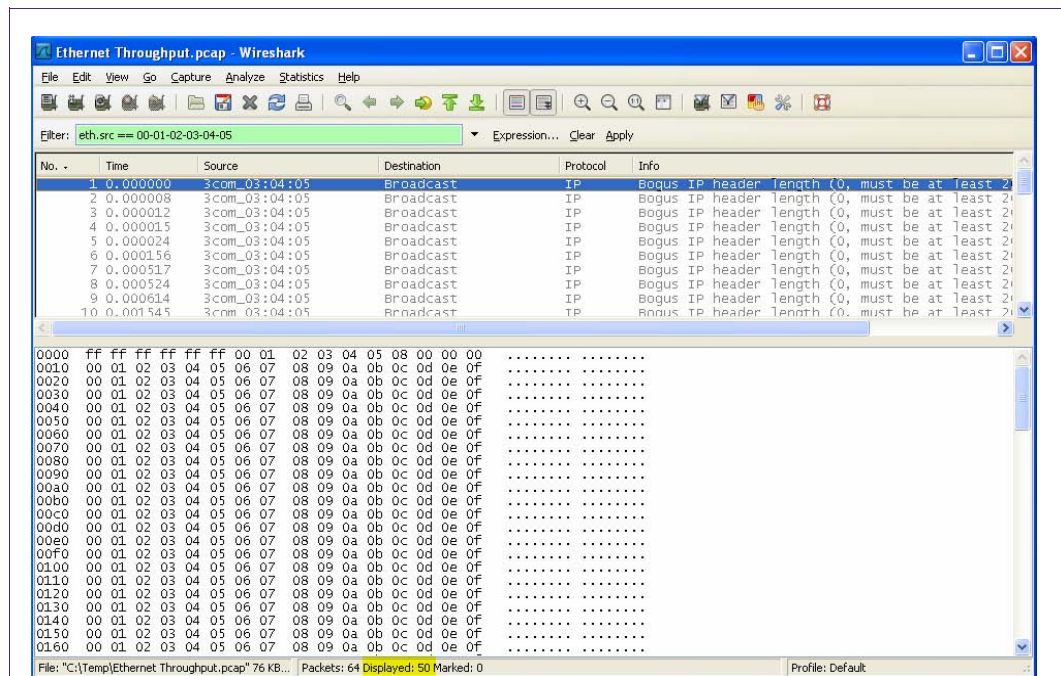
Ethernet mode: Full Duplex – 100 Mbit/s

2.2 Test description

In order to get the maximum Throughput, 50 frames consisting of 1514 B (including Ethernet header), consisting of 75 kB of payload (useful data) will be sent. The CRC (4 B) is automatically added by the EMAC controller (Ethernet controller).

In order to measure the time this process takes, a GPIO pin is set (P0.0 in our case) just before the start of sending the frames and this pin cleared as soon as we finish with the process.

In this way, an oscilloscope can be used to measure the time as the width of the generated pulse at the P0.0 pin. The Board is connected to a PC using an Ethernet cross cable.



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Fig 4. Verifying the data using WireShark

The PC runs a sniffer program (in this case WireShark at <http://www.wireshark.org/>) as a way to verify if the 50 frames were sent and the data is correct. A specific pattern in the payload is used so it can be easily recognized if there is any errors. In the case where the 50 frames arrived at the PC with no errors, the test is considered valid.

2.3 Test scenarios

The EMAC uses a series of Descriptors which provide pointers to memory positions where the data buffers, control and status information reside. In the case of transmission, the frame data should be placed by the application into these data buffers. The EMAC uses DMA to get the user's data and fill the frame's payload before sending it out.

According to the above, the method the application uses in order to copy the application data into those data buffers, will affect the overall measurement of the Throughput. For this reason, three different scenarios are presented:

1. An "Ideal" Scenario, which doesn't consider the application at all;
2. A "Typical" Scenario, where the application copies the application's data into the EMAC's data buffers, using the processor;
3. An "Optimized" Scenario, where the application copies the application's data into the EMAC's data buffers, via DMA.

2.3.1 Scenarios description

1. "Ideal" scenario: In this case, the software sets up the descriptors' data buffers with the test's pattern, and only the TxProduceIndex is incremented 50 times (each for every packet to send) in order to trigger the frame transmission. In other words, the application is not considered at all, and even when this is not a typical user's case, it will provide the maximum possible Throughput in transmission.

2. "Typical" scenario: This case represents the typical case in which the application will copy the data into the descriptors' data buffers before sending the frame. Comparing the results of this case with the previous one, it is apparent that the application is affecting the overall performance. This case should not be considered as the actual EMAC Throughput. However, it is presented here to illustrate how non-optimized applications may lower overall results giving the impression that the hardware is too slow.
3. "Optimized" scenario: This test uses DMA in order to copy the application's data into the descriptors' data buffers. This case considers a real application but using optimized methods which effectively take the advantage of the fast LPC1700 hardware.

2.4 Software

Test software in the form of a Keil MDK project is provided with this application note.

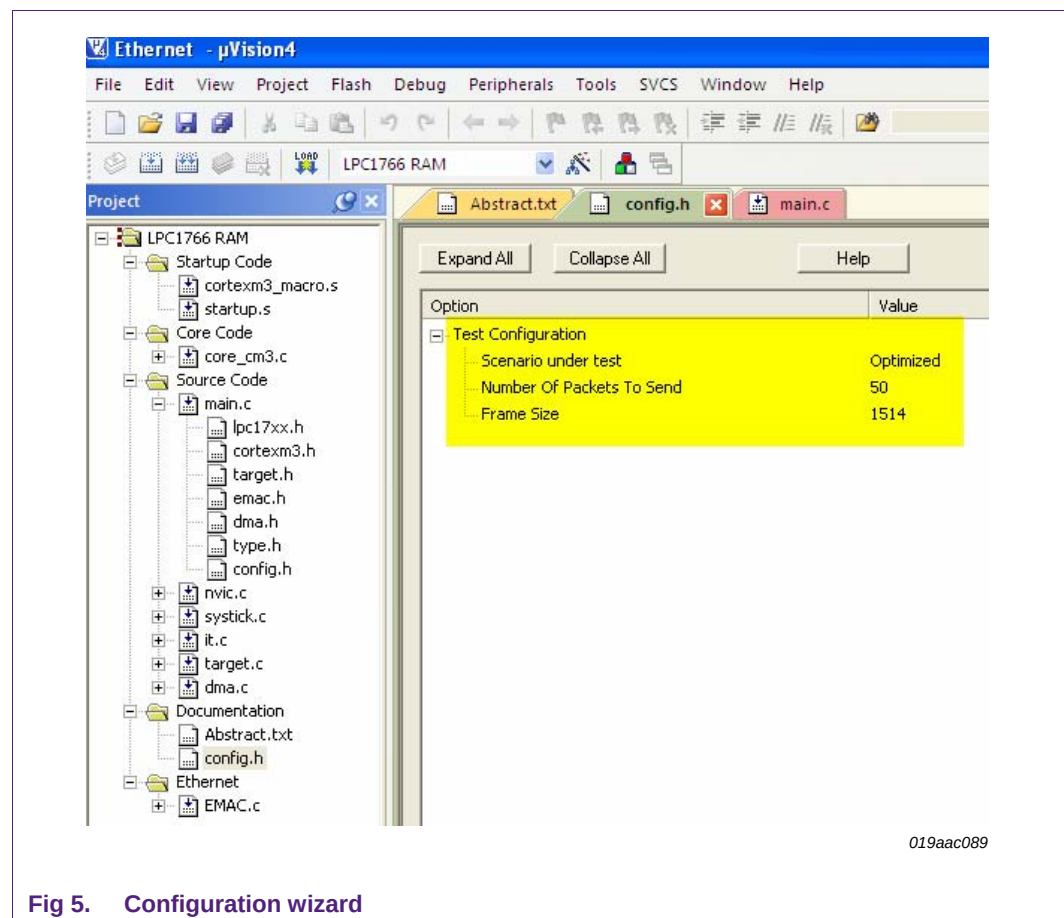


Fig 5. Configuration wizard

The desired scenarios can be selected using the Configuration Wizard opening the "config.h" file.

Besides the scenario, both the Number of Packets to Send and the Frame Size can also be modified through this file.

2.5 Test results

After running the tests, the following results are tabulated:

Table 1. Throughput results

	Frames sent	Payload (Bytes)	Total data (Bytes)	Time (msec)	Throughput (MB/s)	% relative to max possible
Max Possible					12.19	100%
Scenario 1	50	1500	75000	6.25	12.00	98.44%
Scenario 2	50	1500	75000	10.44	7.18	58.93%
Scenario 3	50	1500	75000	7.1	10.56	86.66%

3. Conclusion

Despite the fact that scenario 1 is not a practical case, it provides the maximum value possible for our hardware as a reference, which is very close to the maximum possible for Ethernet at 100 Mbit/s. In scenario 2 the application affects on the overall performance becomes apparent. Finally, scenario 3 shows how an optimized application greatly improves the overall Throughput.

Other ways to optimize the application and get better results were found running the code from Flash (instead from RAM), and in some cases, increasing the number of descriptors.

In summary, Ethernet Throughput is mainly affected by how the application transfers data from the application buffer to the Descriptor's data buffers. Improving this process will enhance the overall Ethernet performance. The LPC1700 and other LPC parts have this optimization built in to the system hardware with DMA support, enhanced EMAC hardware and smart memory bus architecture.

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